---44. The printed circuit board according to claim 1, wherein the electrolytic plated film is formed on the electroless plated film.

45. The printed circuit board according to claim 2, wherein the electrolytic plated film is formed on the electroless plated film.

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46. The method according to claim 6, wherein the electrolytic film is formed on the electroless plated film.

47. The method according to claim 7, wherein the electrolytic film is formed on the electroless plated film.

48. The printed circuit board according to claim 9, wherein the electrolytic film is formed on the electroless plated film.

49. The method according to claim 11, wherein the electrolytic film is formed on the electroless plated film.---

REMARKS

Reconsideration and withdrawal of the rejections of record are respectfully requested.

Summary of Status of Amendments and Office Action

In the present amendment, claims 1-4, 6, 7, 9, 11, 13, 14, 16, 18-23, and 29-43 are amended, claims 44-49 are added, and no claims are cancelled. Therefore, claims 1-49 are pending in the application with claims 1, 2, 6, 7, 9, 11, 13, and 14 being independent.

In the Office Action, claims 1-43 are rejected.

Claims 15, 16, 19-21, 30-32, 35-37, 40, and 41 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, and 35 U.S.C. § 101 as being non-statutory..

Claims 1-43 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,827,604 to UNO et al. (hereinafter "UNO").

Explanation and Support for Amendments

Applicants submit that each of the foregoing amendments is fully supported by the specification. For the convenience of the Examiner, specific examples of support are noted below:

Support for reciting "laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer", is found in present application at, e.g., Figs. 17 and 40. The specification is being amended to provide even more explicit support for this language.

Support for reciting "a roughened layer having a roughened surface formed by etching treatment, polishing treatment, or redox treatment, or having a roughened surface formed by a plated film", is found in the present application at, e.g., the second full paragraph of page 16.

Drawings

The Form PTO-948, attached to the Office Action, indicates that the drawings are objected to as being informal. In response, formal drawings are submitted herewith. Approval thereof is requested.

Declaration

The Office Action objects to the Declaration as having the incorrect filing date for PCT Application No. PCT/JP97/04684. In response, Applicants are filing a corrected Declaration herewith.

In view of the above, Applicants request that this ground of objection be withdrawn.

Specification

In response to the request that the specification be checked for minor errors, Applicants note that the specification is being amended herewith.

In response to the assertion that the application does not contain an Abstract, in contrast with the assertions of the Office Action, Applicants respectfully submit that an Abstract was filed with the application. However, to expedite prosecution, Applicants are filing an Abstract herewith.

In view of the above, Applicants respectfully request that this ground of objection be withdrawn.

Claim Objections

Claim 16 is objected to as reciting "claims" instead of "claim". In response, claim 16 has been amended to recite ---claim---.

Claims 19-21 are objected to as reciting "anyone of" and omitting "as" in claim 21. In response, Applicants note that these informalities were corrected by the Preliminary Amendment filed June 11, 1999 or the Supplemental Preliminary Amendment filed September 20, 1999.

In view of the above, Applicants respectfully request that this ground of objection be withdrawn.

Response to § 112 and § 101 Rejection

Claims 15, 16, 19-21, 30-32, 35-37, 40, and 41 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, and 35 U.S.C. § 101 as being non-statutory. In response, the claims have been amended to even more clearly recite the present invention. In this regard, any amendments to the claims which have been made in this amendment, and which have not been

specifically noted to overcome a rejection based upon the prior art, should be considered to have been intended to clarify the claims and not narrow the claims, such that no estoppel should be deemed to attach thereto.

In this regard, although claims 15 and 16 were rejected, Applicants believe that the Examiner intended to reject claims 13 and 14 based on the reasoning provided in the Office Action.

In view of the above, Applicants respectfully request that this ground of rejection be withdrawn.

Response to § 102 Rejection

Claims 1-43 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,827,604 to UNO et al. (hereinafter "UNO"). The Office Action asserts that UNO teaches a printed circuit board 1 with a conductor circuit or layer comprised of a film 3 and another film 10 and a roughened layer 9 that is a plated layer of copper-nickel-phosphorous alloy, (col. 5, line 23), and the surface is covered with a metal layer having in ionization tendency of more than copper but less than titanium or a noble metal. Concerning claims 6-8, 11, 12, and 27, the Office Action asserts that the method claims are rejected using the same reasoning as applied to the product claims.

In response, Applicants note that independent claim 1 recites a printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit.

Independent claim 2 recites a printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal.

Independent claim 6 recites a method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer.

Independent claim 7 recites a method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal and forming an interlaminar insulating layer.

Independent claim 9 recites a multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer having a roughened surface formed by etching treatment, polishing treatment, or redox treatment, or having a roughened surface formed by a plated film is formed on at least a part of the surface of the underlayer conductor circuit connected to the viahole.

Independent claim 11 recites a method of producing a multilayer printed circuit board comprising forming a lower conductor circuit layer on a surface of a substrate, forming a roughened layer by etching treatment, polishing treatment, redox treatment, or plating treatment on at least a part of the surface of the underlayer conductor circuit connected to a viahole, forming an interlaminar insulating layer thereon, forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the interlaminar insulating layer to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form an upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated film and a viahole.

Independent claim 13 recites a printed circuit board provided with a conductor layer comprising an alignment mark, in which a roughened layer is formed on at least a part of the surface of the conductor layer.

Independent claim 14 recites a printed circuit board provided with a conductor layer comprising an alignment mark, in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

Regarding claims 1 and 2, Applicants respectfully submit that UNO fails to disclose or suggest a printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer. In this regard, UNO discloses a structure which has one interlaminar insulating layer 4 on each side of substrate 2. Therefore, UNO fails to disclose or suggest a printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer.

Concerning independent claim 9, Applicants respectfully submit that UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film. In particular, UNO discloses a copper pattern 3, a roughened layer 9 formed by electroless plating, and another film 10 which may be an electrolytic film, (see Examples 6 and 10). In contrast, the viahole of UNO is formed of copper pattern 6. Thus, UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film.

Even if copper pattern 3, roughened layer 9, and layer 10 are somehow considered to be part of the viahole of UNO, then UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film in combination with a roughened layer . . . formed on at least a part of the surface of the underlayer conductor circuit connected to the viahole. As noted

above, UNO discloses discloses a copper pattern 3, a roughened layer 9 formed by electroless plating, another film 10 which may be an electrolytic film, and a copper pattern 6. If the copper pattern 3, roughened layer 9, and layer 10 are somehow considered to be part of the viahole, then the viahole would not be connected to a roughened layer. Accordingly, UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film in combination with a roughened layer . . . formed on at least a part of the surface of the underlayer conductor circuit connected to the viahole.

For independent claims 13 and 14, Applicants respectfully submit that UNO fails to disclose or suggest an alignment mark. Applicants note that the Office Action fails to explain where UNO discloses an alignment mark. Accordingly, if for any reason this ground of rejection is maintained in a future Office Action, Applicants request further clarification. Furthermore, since the rejection is not clearly set forth, Applicants respectfully submit that if UNO is relied upon in a future Office Action for this ground of rejection, such an Office Action should be made non-final.

Regarding independent method claims 6, 7, and 11, it is again noted that the Office Action asserts that the method claims are rejected using the same reasoning as applied to the product claims. In response, Applicants respectfully submit that the reasoning supporting this rejection is incomplete and inappropriate, because process claims may be separately patentable and especially considering that the Office Action itself asserts that product-by-process claims are directed to the product per se, no matter how actually made. Since the rejection is not clearly set forth, Applicants respectfully submit that if the Examiner relies upon UNO in a future Office Action for this ground of rejection, such an Office Action should be made non-final.

However, to expedite prosecution, Applicants respectfully submit that UNO fails to disclose or suggest etching and removing the electroless plated film beneath the plating resist, as recited in independent claims 6, 7, and 11, or forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer, as recited in independent claim 6. In this regard, UNO discloses forming a plating resist 5 which is formed after the interlaminar insulating layer 4. UNO fails to disclose or suggest etching and removing the electroless plated film beneath the plating resist, as recited in independent claims 6, 7, and 11, or forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer, as recited in independent claim 6.

Additionally, each of the dependent claims under this rejection is patentable over the cited documents at least because each of these dependent claims includes the recitations of independent claim 1, 2, 6, 7, 9, 11, 13, or 14. Moreover, each of the dependent claims under this rejection is patentable over the cited documents because it would not have been obvious to a skilled artisan to incorporate such dependent claim features into the invention as more broadly recited in independent claim 1, 2, 6, 7, 9, 11, 13, or 14.

For instance, new dependent claims 44-49 recite that the electrolytic film is formed on the electroless plated film.

In view of the above, Applicants respectfully request that this ground of rejection be withdrawn.

CONCLUSION

For the reasons advanced above, Applicants respectfully submit that all pending claims patentably define Applicants' invention. Allowance of the application with an early mailing date of the Notices of Allowance and Allowability is therefore respectfully requested.

Should the Examiner have any further comments or questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Motoo ASAI et al.

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MARKED-UP COPY OF AMENDED PARAGRAPHS OF THE SPECIFICATION

Please amend the first full paragraph of page 1 as follows:

---This invention relates to a printed circuit board and a method of producing the same, and more particularly to a printed circuit board which can control the occurrence of cracks in the heat cycle and prevent the dissolution of the conductor circuit caused [in the] by roughening of an interlaminar insulating layer without the degradation of peel strength, and a method of producing the same.---

Please amend the second full paragraph of page 1 as follows:

---Recently, so-called build-up multilayer wiring board [is noticed from a] are in demand for high densification of multilayer wiring boards. This build-up multilayer wiring board is produced, for example, by a method as described in JP-B-4-55555. That is, an insulating agent composed of a photosensitive adhesive for electroless plating is applied onto a core substrate, dried, exposed to a light and developed to form an interlaminar insulating resin layer having openings for viaholes, and then the surface of the interlaminar insulating resin layer is roughened by treating with an oxidizing agent or the like, and a plating resist is formed on the roughened surface, and thereafter a non-forming portion of the plating resist is subjected to an electroless plating to form viaholes and conductor circuits, and then such steps are repeated plural times to obtain a build-up multilayer wiring board.---

Please amend the first full paragraph of page 2 as follows:

---Therefore, if IC chips are mounted on such a wiring board, there is a problem that warping of the board is caused by a difference of thermal expansion coefficient between IC chip and the

insulating resin layer in the heat cycle to concentrate stress into a boundary portion between the plating resist and the conductor circuit due to poor adhesion [property] therebetween and hence cracks are generated in the interlaminar insulating layer contacting with the boundary portion.---

Please amend the third full paragraph on page 2 as follows:

---In the invention of JP-A-6-283860, however, there is no understanding about cracks caused when the heat cycle test is actually carried out after the mounting of IC chips, and only a conductor circuit composed of only an electroless plated film is disclosed. Moreover, when a supplementary test of the heat cycle at –55°C~+125°C is carried out [about the effect] (see Comparative Example 1 as mentioned later), [the occurrence of crack] cracking is not observed in about 1000 cycles, but when the cycle number exceeds 1000 cycles, [the occurrence of crack] cracking is observed.---

Please amend the third full paragraph of page 4 as follows:

---It is [the other] still another object of the invention to provide a method of advantageously producing such a printed circuit board.---

Please amend the second full paragraph of page 5 as follows:

--- (3) [The] A method of producing the multilayer printed circuit board according to the invention comprises [steps of] subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer

on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer [theron] thereon.---

Please amend the paragraph bridging pages 5 and 6 as follows:

---(4) [The] A method of producing the multilayer printed circuit board according to the invention comprises [steps of] subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal and forming an interlaminar insulating layer thereon.---

Please amend the first full paragraph on page 6 as follows:

---In the method described in [the] item (3) or (4), the roughened layer is [preferable to be] preferably formed by plating of copper-nickel-phosphorous alloy.---

Please amend the third full paragraph on page 6 as follows:

---In the printed circuit board described in [the] item (5), the roughened layer is [preferable to be] preferably formed by plating of copper-nickel-phosphorous alloy.---

Please amend the paragraph bridging pages 6 and 7 as follows:

---(6) [The] A method of producing the multiplayer printed circuit board according to the invention comprises [steps of] forming an under layer conductor circuit on a surface of a substrate, forming a roughened layer by an etching treatment, polishing treatment, redox treatment, or a plating treatment on at least a part of a surface of the under layer conductor circuit to be connected to a viahole, forming an interlaminar insulating layer thereon, and forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon and subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form an upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated fim and a viahole.---

Please amend the first full paragraph of page 7 as follows:

---In the method described in [the] item (6), the roughened layer is [preferable to be] preferably formed by plating of copper-nickel-phosphorous alloy.---

Please amend the third full paragraph of page 7 as follows:

---In the printed circuit board described in [the] item (7), the conductor layer is [preferable to be] preferably comprised of an electroless plated film and an electrolytic plated film.---

Please amend the fifth full paragraph of page 7 as follows:

---In the printed circuit board described in [the] item (8), it is preferable that the roughened layer is formed on at least a part of the surface of the conductor layer.---

Please amend the sixth full paragraph of page 7 as follows:

---In the printed circuit board described in [the] item (7) or (8), it is preferable that the alignment mark is an opening portion formed by exposing only the surface of the conductor layer from a solder resist formed on the conductor layer, and it is preferable that a metal layer of nickel-gold is formed on the conductor layer exposed from the opening portion.---

Please amend the last full paragraph of page 7 as follows:

--- Further, in the printed circuit board described in [the] item (7) or (8), it is preferable that the alignment mark is used for positioning to a printed mask, an IC chip mounting and positioning in the mounting of a printed circuit board packaged a semiconductor element to another printed circuit board.---

Please amend the fourth full paragraph of page 8 as follows:

---Fig. 41 is a [partially] <u>partial</u> sectional view showing an alignment mark composed of a conductor layer and used for positioning to a printed mask or an IC chip mounting;---

Please amend the fifth full paragraph of page 8 as follows:

---Fig. 42 is a [partially] <u>partial</u> sectional view showing an alignment mark composed of a conductor layer and used for positioning in the mounting of a printed circuit board packaged a semiconductor element to another printed circuit board; and---

Please amend the second full paragraph of page 9 as follows:

---In such a structure, since the electrolytic plated film is softer and more malleable than the electroless plated film, the conductor circuit is able to follow [to a] size change of the interlaminar insulating resin layer as an upper layer even if warping of the board is generated in the heat cycle. Moreover, in the printed circuit board according to the invention, since the roughened layer is formed on the surface of the conductor circuit, the conductor circuit is strongly adhered to the interlaminar insulating resin layer as an upper layer [and is more easy to follow to a] and more readily follows size change of the interlaminar insulating resin layer.---

Please amend the first full paragraph of page 10 as follows:

--- In such a structure, since the electrolytic plated film is softer and more malleable than the electroless plated film, the viahole is able to follow [to a] size change of the interlaminar insulating resin layer as an upper layer even if a warp of the board is generated in the heat cycle. Moreover, the viahole in the printed circuit board according to the invention is constructed at the inner layer side with the hard electroless plated film and also such an electroless plated film is adhered to the under layer conductor circuit through the roughened layer, so that the viahole is not peeled off from the under layer conductor circuit in the heat cycle. Because the metal layer encroached by the roughened layer is the harder electroless plated film, and hence [the] breakage at the metal layer is [hardly] rarely caused even when [the] peeling force is applied.---

Please amend the last full paragraph of page 10 as follows:

---In short, when the viahole is comprised of only the electrolytic plated film, even if it is adhered to the under layer conductor circuit through the roughened layer, the electrolytic plated film itself is soft and is apt to peel off due to the heat cycle. While, when the viahole is comprised of only the electroless plated film, it can not follow [to the] size change of the interlaminar insulating resin layer and hence [the crack] cracking is caused in the interlaminar insulating resin layer [existing] on the viahole. In the printed circuit board according to the invention, the viahole is comprised of the electrolytic plated film and the electroless plated film and connected to the under layer conductor circuit through the roughened layer, so that the occurence of cracks generated in the interlaminar insulating resin layer on the viahole, and [the] peeling between the viahole and the under layer conductor circuit in the heat cycle can be prevented at the same time.---

Please amend the first full paragraph of page 11 as follows:

---Moreover, when the interlaminar insulating resin layer is roughened, it is desirable that a plated film encroached into the roughened layer is hard. Because [the] breakage is [hardly] rarely caused at the plated film portion when [the] peeling force is applied.---

Please amend the second full paragraph of page 11 as follows:

---In [the] structure ②, the roughened layer may be formed on the surface of the viahole. Because the roughened layer is strongly adhered to the interlaminar insulating resin layer as an upper layer and hence the viahole is more [easy] able to follow [to the] size change of the interlaminar insulating resin layer. Further, the roughened layer on the under layer conductor circuit may be

formed on not only the portion connecting to the viahole but also the whole surface of the under layer conductor circuit. [Because the adhesion property] The adhesion of the under layer conductor circuit to the interlaminar insulating resin layer is improved [likewise] like the above structure ①.---

Please amend the third full paragraph of page 11 as follows:

---In [the] structure ②, it is desirable that the under layer conductor circuit connecting to the viahole is comprised of the electrolytic plated film and the electroless plated film, and the electroless plated film is located at an inner layer side and the electrolytic plated film is located at an outer layer side. Because the inner layer side of the under layer conductor circuit is adhered to the interlaminar insulating resin layer, [so that] it is [desirable to be] desirably a hard electroless plated film in order to ensure peel strength, while the contrary side is connected to the viahole and is [desirable to be] desirably an electrolytic plated film having an excellent following property to [the] size change.---

Please amend the last full paragraph of page 12 as follows:

---In such a structure, since the electrolytic plated film is softer and more malleable than the electroless plated film, the conductor layer is able to follow [to the] size change of the solder resist layer as an upper layer even if warping of the board is generated in a heat cycle. Moreover, when the roughened layer is formed on the surface of the conductor layer, the conductor layer is strongly adhered to the solder resist layer as an upper layer and is [easy] able to follow [to the] size change of the solder resist layer. Further, the conductor contacting with the interlaminar insulating layer is an electroless plated film and high in the hardness, and hence [a] peel strength can be increased.---

Please amend the second full paragraph of page 13 as follows:

---In [the structure ③, ④,] structures ③ and ④, it is further desirable that the metal layer made of nickel-gold is formed on the conductor layer as an alignment mark exposed from the opening portion. Because gold is high in [the] reflectance and advantageously functions as an alignment mark. The metal layer made of nickel-gold may be formed by electroless plating. For example, the nickel layer is comprised of a nickel plated film having a thickness of 5μm, and the gold layer is comprised of a flash gold plated film having a thickness of 0.1μm or a thick gold plated film having a thickness of 0.5μm.---

Please amend the paragraph bridging pages 13 and 14 as follows:

---In [the structure ③, ④,] structures ③ and ④, as shown in Fig. 41, the printed circuit board is comprised, for example, of an insulating substrate 1, a first layer conductor circuit 4 and an interlaminar insulating layer 2 (an adhesive layer for electroless plating) formed thereon, a pad (a conductor pattern) 21 for a solder bump formation [composing] comprising a part of a second layer conductor circuit, an alignment mark 18 for positioning to a printed mask and an alignment mark 19 for an IC chip mounting formed on the interlaminar insulating agent 2 through semi-additive process, a solder resist layer 14 formed on a portion other than the alignment mark 18, 19 and the pad 21 for the solder bump formation. The alignment mark 18 for positioning to the printed mask is formed on a portion forming no conductor pattern in the vicinity of an outer peripheral portion of the printed circuit board. Concretely, it is formed, for example, on an outside of a product portion A shown in Fig. 41. Therefore, the alignment mark 19 for the IC chip mounting enables an IC chip mounting

without influence of the mark 18. In this case, the vicinity of the outer peripheral portion means an outside portion of the product portion as above mentioned. Further, the alignment mark 19 for the IC chip mounting is formed on each product portion in the printed circuit boards in order to mount an IC chip on each product portion. Further, in case of mounting a semiconductor element to produce a packaged board, the alignment mark 20 used for mounting the packaged board to another printed circuit board is formed on the innermost side as shown Fig. 42. The alignment mark 20 is [desirable to be] desirably a cross-shaped mark as shown Fig. 43. In case of adopting the cross-shaped mark, an opening of a solder resist layer is formed so as to cover the peripheral edge of the cross.---

Please amend the first full paragraph of page 14 as follows:

---Particularly, the alignment marks 18, 19 are [preferable to be] preferably formed in the opening portions exposing only the surface of the conductor layer from the solder resist layer formed on the conductor layer (including the viahole). Because the peripheral edge of the conductor layer overlaps with the solder resist layer and hence the peeling of the conductor can be prevented by holding the conductor with the solder resist layer as shown Fig. 41. Moreover, in the heat cycle, cracks generated starting from the boundary portion between the conductor layer and the interlaminar insulating resin layer due to the difference of thermal expansion coefficient can be controlled.---

Please amend the second full paragraph of page 14 as follows:

---Particularly, the alignment mark for positioning to a printed mask has [a] the following effect.---

Please amend the first full paragraph of page 15 as follows:

---If the conductor layer as an alignment mark is perfectly exposed, since a center of the conductor is recognized as the central position of the alignment mark in a camera, [the] position shifting of the opening in the solder resist layer cannot be recognized. As a result, the opening portion of the printed mask is not coincident with the opening portion of the solder resist layer, so that an opening volume of the printed mask is decreased due to the solder resist layer and the height of a solder bump [become] <u>becomes</u> low.---

Please amend the second full paragraph of page 15 as follows:

---On the other hand, if the peripheral edge of the conductor layer as an alignment mark is covered with the solder resist layer, since a center of the conductor exposed from the opening portion is recognized as the central position of the alignment mark in a camera, even if the photomask for opening the solder resist layer is shifted to cause [the] position shifting of the opening in the solder resist layer, the alignment mark is shifted [to] <u>in</u> the same direction and amount as mentioned above. As a result, the opening portion of the printed mask is coincident with the opening portion of the solder resist layer, so that an opening volume of the printed mask is not decreased due to the solder resist layer and the height of a solder bump is not [lowed] <u>lowered</u>.---

Please amend the paragraph bridging pages 15 and 16 as follows:

---As mentioned above, in the above structures ①, ②, ④ of the printed circuit board according to the invention, the inner layer side of the conductor is constructed with the electroless plated film <u>which is</u> harder than the electrolytic plated film, and hence the peel strength is never

lowered. Because the higher the hardness of the portion contacting with an interlaminar insulating layer and located in the inner layer side of the conductor circuit (in case of adopting an adhesive for electroless plating as mentioned later as an interlaminar insulating layer, the portion contacting with a roughened surface), the higher the peel strength. Even when the printed circuit board according to the invention is mounted with an IC chip and subjectrd to a heat cycle test under –55°C~+125°C, the occurrence of cracks generated in the interlaminar insulating resin layer starting from the conductor circuit or the viahole, and cracks generated in the solder resist layer starting from the boundary between the side face of the conductor layer and the solder resist layer contacting therewith can be prevented, and also the peeling of the conductor circuit, the viahole or the solder reist layer is not observed.---

Please amend the paragraph bridging pages 16 and 17 as follows:

---Particularly, it is desirable that the roughened layer is an alloy layer composed of copper-nickel-phosphorus. Because the alloy layer is a needle-shaped crystal layer and is excellent in [the] adhesion [property] to the solder resist layer. Further, the alloy layer is electrically conductive, and hence even if the solder body is formed on the surface of the pad, the removal of the alloy layer is not necessary.---

Please amend the first full paragraph of page 17 as follows:

---The composition of the alloy layer is [desirable to be] <u>desirably</u> 90-96 wt% of copper, 1-5 wt% of nickel and 0.5-2 wt% of phosphorus because the needle-shaped structure is obtained in such a composition ratio.---

Please amend the fifth full paragraph of page 17 as follows:

---The roughened layer formed on the surface of the conductor circuit [is desirable to have] desirably has a thickness of 0.5-10 μm, preferably 0.5-7μm. Because, if the thickness is too thick, the roughened layer itself is apt to be damaged and peeled, while if it is too thin, [the] adhesion [property lowers] is lowered.---

Please amend the paragraph bridging pages 17 and 18 as follows:

---In the invention, the electroless plated film constituting the conductor circuit [is desirable to have] desirably has a thickness of 0.1-5μm, preferably 0.5-3μm. Because, if the thickness is too thick, the [following property to] ability to follow the interlaminar insulating resin layer lowers, while if it is too thin, [the] degradation of peel strength is caused and [the] electric resistance becomes large in the case of being subjected to an electrolytic plating to cause [the] scattering in the thickness of the plated film.---

Please amend the first full paragraph of page 18 as follows:

---Furthermore, the electrolytic plated film constituting the conductor circuit [is desirable to have] desirably has a thickness of 5-30μm, preferably 10-20μm. Because, if the thickness is too thick, [the] degradation of peel strength is caused, while if it is too thin, the [following property to] ability to follow the interlaminar insulating resin layer lowers.---

Please amend the second full paragraph of page 18 as follows:

---Thus, in the invention, the conductor circuit is comprised of the electrolytic plated film and the electroless plated film, and the roughened layer formed on the surface of the conductor

circuit mainly contacts with the electrolytic plated film. The electrolytic plated film is apt to be dissolved by [the] local electrode reaction as [comparede] compared with the electroless plated film, so that when the electrolytic plated film forms the local electrode with the roughened layer, it is rapidly dissolved and hence a large hole is apt to be formed in the surface of the conductor circuit. In the invention, therefore, it is particularly desirable that the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal, which is another feature in this point. Thus, the dissolution of the conductor circuit through the local electrode reaction can be [controled] controlled.

Please amend the second paragraph of page 19 as follows:

---Such a metal or noble metal layer [is desirable to have] desirably has a thickness of 0.1-2μm.---

Please amend the third full paragraph of page 19 as follows:

---Among such a metal or noble metal, tin is preferable. Tin can form a thin layer through an electroless substitution plating and can advantageously follow [to] the roughened layer.---

Please amend the second full paragraph of page 21 as follows:

---The roughened layer is formed by an electroless plating. The composition of the electroless plating aqueous solution [is desirable to have] desirably has a copper ion concentration of 2.2×10^{-2}~4.1×10^{-2} mol/l, a nickel ion concentration of 2.2×10^{-3}~4.1×10^{-3} mol/l and a hypophosphorus acid ion concentration of 0.20~0.25 mol/l.---

Please amend the third full paragraph of page 21 as follows:

---The film deposited within the above range [is] has a needle in [the] crystal structure and is excellent in the anchor effect. The electroless plating aqueous solution may be added with a complexing agent and additives in addition to the above compounds.---

Please amend the fifth full paragraph of page 21 as follows:

---Moreover, through-holes are formed in the core substrate, and the front and back wiring layers may be electrically [be] connected to each other through the through-holes.---

Please amend the seventh full paragraph of page 21 as follows:

---(2) Then, an interlaminar insulating resin layer is formed on the printed wiring substrate prepared in [the] step (1).---

Please amend the first full paragraph of page 22 as follows:

---(3) After the adhesive layer for electroless plating formed in [the] step (2) is dried, an opening portion for the formation of viahole is formed, if necessary.---

Please amend the second full paragraph of page 22 as follows:

---The opening portion for the formation of viahole is formed in the adhesive layer by light exposure, development and thermosetting in the case of [the] photosensitive resin, or by thermosetting and laser working in the case of [the] thermosetting resin (see Fig. 6).---

Please amend the fourth full paragraph of page 22 as follows:

---As the acid, there are phosphoric acid, hydrochloric acid, sulfuric acid, and an organic acid such as formic acid, acetic acid or the like. Particularly, the use of the organic acid is desirable because [when] it hardly corrodes the metal conductor circuit exposed from the viahole by the roughening treatment.---

Please amend the fourth full paragraph of page 24 as follows:

--- In the case of tin, a solution of tin borofluoride-thiourea or tin chloride-thiourea is used. In this case, Sn layer having a thickness of about 0.1~2μm is formed through Cu-Sn substitution reaction.---

Please amend the fifth full paragraph of page 24 as follows:

---In the case of the noble metal, there may be adopted sputtering method, vaporization method and the like.---

Please amend the seventh full paragraph of page 24 as follows:

---(11) Then, an upper layer conductor circuit is formed by repeating [the] steps (3)-(8)(see Figs. 14-17). In this case, a roughened layer may be formed on the surfaces of the conductor circuits in the same manner as in the step (9), and it is particularly desirable that the roughened layer is formed on the surface of the conductor layer serving as an alignment mark and a pad for a solder bump formation. In view of the above, the printed circuit board may be formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer.---

Please amend the second full paragraph of page 25 as follows:

---The opening size of the opening portion coresponding to the pad portion for the solder bump formation may be made larger than the diameter of the pad to completely expose the pad or may be made smaller than the diameter of the pad so as to cover the peripheral edge of the pad with the solder resist. Particularly, when the opening size is smaller than the diameter of the pad, the roughened layer on the pad surface is closely adhered to the solder resist, so that the pad can be restrained by the solder resist to prevent [the] peeling of the pad. On the other hand, the conductor layer serving as the alignment mark is covered at its peripheral edge with the solder resist so as not to completely expose the opening portion of the solder resist layer.---

Please amend the third full paragraph of page 26 as follows:

---Further, bisphenol [F-type] F epoxy resin is filled between the innerlayer conductor circuits 4 and in the through-holes 9 (see Fig. 3).---

Please amend the paragraph bridging pages 26 and 27 as follows:

---(2) The substrate treated in [the] step (1) is washed with water, dried, acidically degreased and soft-etched. Then, the substrate is treated with a catalyst solution comprising palladium chloride and organic acid to give a Pd catalyst, which is activated and subjected to a plating in an electroless plating bath comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having pH=9 to form a roughened layer 11 (uneven layer) of Cu-Ni-P alloy having a thickness of 2.5μm on the surface of the copper conductor circuits 4 (see Fig. 4).---

Please amend the first full paragraph of page 27 as follows:

---(3) A photosensitive adhesive solution (interlaminar resin insulating agent) is prepared by mixing 70 parts by weight of 25% acrylated product of cresol novolac [type] epoxy resin (made by Nippon Kayaku Co., Ltd. molecular weight: 2500) dissolved in DMDG (diethylene glycol dimethyl ether), 30 parts by weight of polyether sulphone (PES), 4 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co., Ltd. trade name: 2E4MZ-CN), 10 parts by weight of caprolacton-modified tris(acroxyethyl) isocyanurate (made by Toa Gosei Co., Ltd. trade name: Aronix M325) as a photosensitive monomer, 5 parts of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator, 0.5 parts by weight of [Micheler s] Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and 35 parts by weight at 5.5μm on average and 5 parts by weight at 0.5μm on average of epoxy resin particles, adding NMP (normal methyl pyrolidone), adjusting a viscosity to 12 [Pa s] Pa· s in a homodisper agitating machine and kneading them through three rolls.

Please amend the second full paragraph of page 27 as follows:

---(4) The photosensitive adhesive solution obtained in [the] step (3) is applied onto both surfaces of the substrate treated in [the] step (2) by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60°C for 30 minutes to form an adhesive layer 2 having a thickness of [60μ m] 60μm (see Fig. 5).

Please amend the third full paragraph of page 27 as follows:

---(5) A photomask film depicted with viaholes is adhered onto each surface of the substrate provided with the adhesive layer 2 in [the] step (4) and exposed by irradiation of ultraviolet ray.---

Please amend the paragraph bridging pages 27 and 28 as follows:

---(6) The substrate exposed in [the] step (5) is developed by spraying DMTG (triethylene glycol dimethylether) solution to form openings for viaholes of 100 μmφ in the adhesive layer 2. Further, the substrate is exposed to a superhigh pressure mercury lamp at 3000 mJ/cm^2 and then heated at 100°C for 1 hour and at 150°C for 5 hours to form an adhesive layer 2 of 50μm in thickness having the openings (opening 6 for the formation of viahole) with an excellent size accuracy corresponding to the photomask film (see Fig. 6). Moreover, the roughened layer 11 is partially exposed in the opening 6 for the viahole.---

Please amend the first full paragraph of page 28 as follows:

---(7) The substrate provided with the openings 6 for the viaholes in [the] steps (5), (6) is immersed in chromic acid for 2 minutes to dissolve and remove epoxy resin particles from the surface of the adhesive layer, whereby the surface of the adhesive layer 2 is roughened. Thereafter, it is immersed in a neutral solution (made by Shipley) and washed with water (see Fig. 7).---

Please amend the second full paragraph of page 28 as follows:

---(8) A palladium catalyst (made by Atotec Co., Ltd.) is applied to the substrate subjected to a roughening treatment (roughening depth: 5μm) in [the] step (7) to give a catalyst nucleus to the surface of the adhesive layer 2 and the opening 6 for the viahole.---

Please amend the first full paragraph of page 29 as follows:

---(10) A commercially available photosensitive dry film is attached to the electroless copper plated film 12 formed in [the] step (9) and a photomask film is placed on the dry film, which is exposed to a light at 100 mJ/cm^2 and developed with a solution of 0.8% sodium carbonate to form a plating resist 3 having a thickness of 15μm (see Fig. 9).---

Please amend the last full paragraph of page 29 as follows:

---(12) After the plating resist 3 is peeled and removed with 5% KOH, the electroless plated film 12 beneath the plating resist 3 is dissolved and removed by etching with a mixed solution of sulfuric acid and hydrogen peroxide to form conductor circuits 5 (including viaholes 7) of 18 [m] μm in thickness comprised of the electroless copper plated film 12 and the electrolytic copper plated film 13 (see Fig. 11).---

Please amend the second full paragraph of page 30 as follows:

---(14) [The steps] Steps (4)-(12) are repeated to further form [an] upper layer conductor circuits (including viaholes and alignment marks) to thereby produce a wiring substrate (see Figs. 13-17).---

Please amend the third full paragraph of page 30 as follows:

---(15) On the other hand, a solder resist composition is prepared by mixing 46.67 g of a photosensitized oligomer (molecular weight: 4000) in which 50% of epoxy group in 60% by weight of cresol novolac [type] epoxy resin (made by Nippon Kayaku Co., Ltd.) dissolved in DMDG is acrylated, 15.0 g of 80% by weight of bisphenol [A-type] A epoxy resin (made by Yuka Shell Co., Ltd. trade name: Epikote 1001) dissolved in methyl ethyl ketone, 1.6 g of an imidazole curing agent (made by Shikoku Kasei Co., Ltd. trade name: 2E4MZ-CN), 3 g of a polyvalent acrylic monomer (made by Nippon Kayaku Co., Ltd. trade name: R604) as a photosensitive monomer, 1.5 g of a polyvalent acrylic monomer (made by Kyoeisha Kagaku Co., Ltd. trade name: DPE6A), 0.71 g of a dispersion type deforming agent (made by Sannopuko Co., Ltd. trade name: S-65), 2 g of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator and 0.2 g of Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and adjusting a viscosity to 2.0 Pa· s at 25°C.---

Please amend the second full paragraph of page 31 as follows:

---(16) The above solder resist composition is applied onto the wiring substrate obtained in [the] step (14) at a thickness of 20μm. Then, the substrate is dried at 70°C for 20 minutes and at 70°C for 30 minutes and a photomask film is placed thereon and then exposed to [an] ultraviolet [ray] rays at 1000 mJ/cm^2 and developed with DMTG. Further, it is heated at 80°C for 1 hour, at 100°C for 1 hour, at 120°C for 1 hour and at 150°C for 3 hours to form a solder resist layer 14 (thickness: 20μm) opened in the pad portion (opening size: 200μm).---

Please amend the second full paragraph of page 32 as follows:

---A multilayer printed circuit board having solder bumps is produced in the same manner as in Example 1 except that the roughening of the conductor circuit is carried out by etching. In this case, an etching solution of Durabond (trade name, made by Meck Co., Ltd.) is used. Further, an Au layer having a thickness of 0.5μm is formed on the surface of the roughened layer by [spputtering] sputtering.---

Please amend the last full paragraph of page 32 as follows:

---①. 35 parts by weight of a resin solution obtained by dissolving 25% acrylated product of cresol novolac [type] epoxy resin (made by Nippon Kayaku Co., Ltd. molecular weight: 2500) in DMDG at a concentration of 80 wt% is mixed with 3.15 parts by weight of a photosensitive monomer (made by Toa Gosei Co., Ltd. trade name: Aronix M315), 0.5 parts by weight of a defoaming agent (made by Sannopuko Co., Ltd. trade name: S-65) and 3.6 parts by weight of NMP with stirring.---

Please amend the fifth full paragraph of page 33 as follows:

---①. 35 parts by weight of a resin solution obtained by dissolving 25% acrylated product of creasol novolac [type] epoxy resin (made by Nippon Kayaku Co., Ltd. molecular weight: 2500) in DMDG at a concentration of 80 wt% is mixed with 4 parts by weight of a photosensitive monomer (made by Toa Gosei Co., Ltd. trade name: Aronix M315), 0.5 parts by weight of a defoaming agent (made by Sannopuko Co., Ltd. trade name: S-65) and 3.6 parts by weight of NMP with stirring.---

Please amend the second full paragraph of page 34 as follows:

---①. 100 parts by weight of bisphenol [F-type] F epoxy monomer (made by Yuka Shell Co., Ltd. trade name: YL983U, molecular weight: 310), 170 parts by weight of SiO_2 spherical particles having an average particle size of 1.6μm and coated on its surface with a silane coupling agent (made by Adomatic Co., Ltd. trade name: CRS 1101-CE, the maximum size of the particles is not more than the thickness (15 [m] μm) of innerlayer copper pattern as mentioned below) and 1.5 parts by weight of a leveling agent (made by Sannopuko Co., Ltd. trade name: Perenol S4) are kneaded through three rolls and a viscosity thereof is adjusted to 45,000-49,000 cps at 23±1°C.---

Please amend the third full paragraph of page 35 as follows:

---(4) The one-side surface of the substrate treated in [the] step (3) is polished by a belt sander polishing using #600 belt polishing paper (made by Sankyo Rikagaku Co., Ltd.) in such a manner that the resin filler is not left on the surface of the innerlayer copper pattern 4 or the land surface of the through-hole 9, and then buff-polished so as to remove scratches formed by the belt sander polishing. Such a series of polishings is applied to the other surface of the substrate.---

Please amend the first full paragraph of page 36:

---(5) A roughened layer (uneven layer) 11 of Cu-Ni-P alloy having a thickness of 2.5μm is formed on the exposed surfaces of the innerlayer conductor circuit 4 and the land of the through-hole 9 [in the] of step (4) and further a Sn layer having a thickness of 0.3 [m] μm is formed on the surface of the roughened layer 11 (see Fig. 25, provided that the Sn layer is not shown).---

Please amend the first full paragraph of page 37 as follows:

---(6) The interlaminar insulating resin material of [the] item B (viscosity: 1.5 [Pa s] Pa· s) is applied onto both surfaces of the substrate treated in [the] step (5) by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60°C for 30 minutes (pre-baking) to form an insulating layer 2a.---

Please amend the second full paragraph of page 37 as follows:

---Further, the adhesive for electroless plating of [the] item A (viscosity: 7 [Pa s] Pa· s) is applied onto the insulating layer 2a by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60°C for 30 minutes (pre-baking) to form an adhesive layer 2b (see Fig. 26).---

Please amend the third paragraph of page 37 as follows:

---(7) A photomask film depicted with black circles of 85 μm in diameter is closely adhered onto both surfaces of the substrate provided with the insulating layer 2a and the adhesive layer 2b in [the] step (6) and exposed to a superhigh pressure mercury lamp at 500 mJ/cm^2. It is developed by spraying DMTG solution and further exposed to a superhigh pressure mercury lamp at 3000 mJ/cm^2 and heated at 100°C for 1 hour and at 150°C for 5 hours (post baking) to form an interlaminar insulating resin layer (two-layer structure) of 35μm in thickness having openings of 85 μm in diameter (openings 6 for the formation of viaholes) with an excellent size accuracy corresponding to the photomask film (see Fig. 27). Moreover, the tin plated layer is partially exposed in the opening for viahole.---

Please amend the third full paragraph of page 38 as follows:

---(10) A commercially available photosensitive dry film is adhered to the electroless copper plated film 12 formed in [the] step (9) and a mask is placed thereon and exposed to a light at 100 mJ/cm^2 and developed with 0.8% of sodium carbonate to form a plating resist 3 having a thickness of 15 μm (see Fig. 30).---

Please amend the second full paragraph of page 40 as follows:

---(14) [The steps] Steps (6)-(13) are repeated to further form upper layer conductor circuits (including viaholes and alignment marks) to thereby produce a multilayer wiring substrate. However, Sn substitution is not conducted (see Figs. 34-39).---

Please amend the third full paragraph of page 40 as follows:

---(15) On the other hand, a solder resist composition is prepared by mixing 46.67 g of a photosensitized oligomer (molecular weight: 4000) in which 50% of epoxy group in 60% by weight of cresol novolac [type] epoxy resin (made by Nippon Kayaku Co., Ltd.) dissolved in DMDG is acrylated, 15.0 g of 80% by weight of bisphenol [A-type] A epoxy resin (made by Yuka Shell Co., Ltd. trade name: Epikote 1001) dissolved in methyl ethyl ketone, 1.6 g of an imidazole curing agent (made by Shikoku Kasei Co., Ltd. trade name: 2E4MZ-CN), 3 g of a polyvalent acrylic monomer (made by Nippon Kayaku Co., Ltd. trade name: R604) as a photosensitive monomer, 1.5 g of a polyvalent acrylic monomer (made by Kyoeisha Kagaku Co., Ltd. trade name: DPE6A), 0.71 g of a dispersion type deforming agent (made by Sannopuko Co., Ltd. trade name: S-65), 2 g of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator and 0.2 g of Micheler's ketone

(made by Kanto Kagaku Co., Ltd.) as a photosensitizer and adjusting a viscosity to 2.0 Pa·s at 25°C.--

Please amend the first full paragraph of page 41 as follows:

---(16) The above solder resist composition is applied onto both surfaces of the multilayer wiring substrate obtained in [the] step (14) at a thickness of 20 μm. Then, the substrate is dried at 70°C for 20 minutes and at 70°C for 30 minutes and a photomask film of 5 mm in thickness depicted with a circle pattern (mask pattern) is placed thereon and then exposed to [an] ultraviolet [ray] rays at 1000 mJ/cm^2 and developed with DMTG. Further, it is heated at 80°C for 1 hour, at 100°C for 1 hour, at 120°C for 1 hour and at 150°C for 3 hours to form a solder resist layer 14 (thickness: 20 μm) opened in the pad portion (including viahole and its land portion, opening size: 200 [m] μm).---

Please amend the first full paragraph of page 43 as follows:

---(6-8) The substrate is immersed in an aqueous solution of lead oxide (3.75 g/l), sodium cyanide (26.3 g/l) and sodium hydroxide (105 g/l) as an electroless plating aqueous solution to [deposite] deposit on the surface of the roughened layer.---

Please amend the fourth full paragraph of page 43 as follows:

---A dry film photo-resist is laminated on the substrate treated in [the step] steps (1)-(8) of Example 1, and exposed and developed to form a plating resist. Then, after [the] step (9) of Example 1 is carried out, the plating resist is peeled and removed in the same manner as in [the] step (12) and the whole surface of the conductor circuit is roughened by [the] step (13) of Example 1.

Thereafter, the formation of interlaminar insulating resin layer, roughening treatment, the formation of plating resist and electroless copper plating are carried out in the same manner as in Example 1, and after the plating resist is peeled and removed, a multilayer printed circuit board having solder bumps is produced by carrying [the] out steps (15)-(19) of Example 1.---

Please amend the first full paragraph of page 44 as follows:

--- A multilayer printed circuit board having solder bumps is produced in the same manner as in Example 1 except that after the roughening of the conductor circuit, Cu-Sn substitution reaction is carried out by immersing in a solution of 0.1 mol/l of tin borofluoride and 1.0 mol/l of thiourea at a temperature of [50 C] 50°C and pH=1.2 to form a Sn layer having a thickness of 0.3 μm on the surface of the roughened layer (the Sn layer is not shown).---

Please amend the second full paragraph of page 44 as follows:

---After IC chip is mounted onto each of the printed circuit boards of the Examples and Comparative Examples, heat cycle tests of 1000 cycles and 2000 cycles under conditions of –55°C for 15 minutes, room temperature for 10 minutes and 125°C for 15 minutes are carried out.---

Please amend the fourth full paragraph of page 44 as follows:

---The results are shown in Table 1. As seen from the results of this table, the occurrence of [crack] cracks is not observed at about 1000 cycles in the Examples and Comparative Examples, while the occurrence of [crack] cracks is observed at 2000 cycles in the Comparative Examples. Further, the peel strength is [indicated to be] equal or higher [value as compared with] than that of the conductor circuit comprised of only an electroless plated film.---

MARKED-UP COPY OF CHANGES TO CLAIMS:

1. (Amended) A printed circuit board formed by laminating [an] a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, [characterized in that] wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer [is formed] on at least a part of the surface of the conductor circuit.

2. (Amended) A printed circuit board formed by laminating [an] a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, [characterized in that] wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer [is formed] on at least a part of the surface of the conductor circuit, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal.

3. (Twice Amended) A printed circuit board according to claim 1, wherein the roughened layer is [formed] on at least a part of the surface inclusive of a side surface of the conductor circuit.

4. (Three Times Amended) A printed circuit board according to claim 1, wherein the roughened layer is [formed] on at least a part of a side face of the conductor circuit.

6. (Amended) A method of producing a multilayer printed circuit board comprising [steps of] subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing

the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer.

7. (Amended) A method of producing a multilayer printed circuit board comprising [steps of] subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal and forming an interlaminar insulating layer.

9. (Amended) A multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer <u>having a roughened surface formed by etching treatment, polishing treatment, or redox treatment, or having a roughened surface formed by a plated film</u> [is formed] on at least a part of the surface of the underlayer conductor circuit connected to the viahole.

11.(Amended) A method of producing a multilayer printed circuit board comprising [steps of] forming a lower conductor circuit layer on a surface of a substrate, forming a roughened layer by etching treatment, polishing treatment, redox treatment, or plating treatment on [a surface of the substrate] at least a part of the surface of the underlayer conductor circuit connected to a viahole, forming an interlaminar insulating layer thereon, forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the [substrate] interlaminar insulating layer to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form an upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated film and a viahole.

13. (Amended) A printed circuit board provided with a conductor layer [used as] comprising an alignment mark, in which a roughened layer is formed on at least a part of the surface of the conductor layer.

14. (Amended) A printed circuit board provided with a conductor layer [used as] comprising an alignment mark, in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

16. (Twice Amended) A printed circuit board according to [claims] claim 15, wherein a metal layer of nickel-gold is [formed] on the conductor layer exposed from the opening portion.

18. (Amended) A printed circuit board according to claim 14, wherein the roughened layer is [formed] on at least a part of the surface of the conductor layer.

19. (Twice Amended) A printed circuit board according to claim 13, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

20. (Twice Amended) A printed circuit board according to claim 13, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

21. (Three Times Amended) A printed circuit board according to claim 13, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

22. (Amended) A printed circuit board according to claim 2, wherein the roughened layer is [formed] on at least a part of the surface inclusive of a side surface of the conductor circuit.

23. (Amended) A printed circuit board according to claim 2, wherein the roughened layer is [formed] on at least a part of a side face of the conductor circuit.

29. (Amended) A printed circuit board according to claim 14, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

30. (Amended) A printed circuit board according to claim 15, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

31. (Amended) A printed circuit board according to claim 16, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

32. (Amended) A printed circuit board according to claim 17, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

33. (Amended) A printed circuit board according to claim 18, [wherein the alignment mark is used for] which is made by a process comprising positioning [to] a printed mask relative to the alignment mark.

34. (Amended) A printed circuit board according to claim 14, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

35. (Amended) A printed circuit board according to claim 15, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

36. (Amended) A printed circuit board according to claim 16, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

37. (Amended) A printed circuit board according to claim 17, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

38. (Amended) A printed circuit board according to claim 18, [wherein the alignment mark is used for] which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

39. (Amended) A printed circuit board according to claim 14, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

40. (Amended) A printed circuit board according to claim 15, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

41. (Amended) A printed circuit board according to claim 16, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

42. (Amended) A printed circuit board according to claim 17, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

43. (Amended) A printed circuit board according to claim 18, [wherein the alignment mark is used for] which is made by a process comprising positioning [during mounting of] a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

---Abstract of the Disclosure

A printed circuit board is by formed by laminating an interlaminar insulating layer on a conductor circuit of a substrate, in which the conductor circuit includes an electroless plated film and an electrolytic plated film and a roughened layer is formed on at least a part of the surface of the conductor circuit.---